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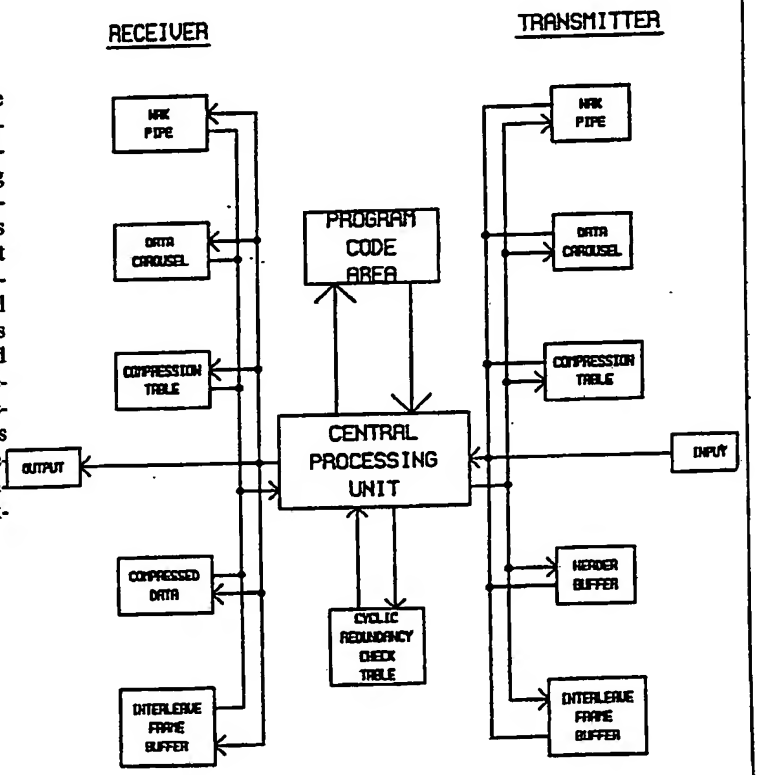
(54) Title: METHOD AND SYSTEM FOR DATA TRANSMISSION, USING FORWARD ERROR CORRECTION AND FRAME INTERLEAVING


(57) Abstract

A method of operating a high speed, error-free data transmission system in a noisy medium comprises compressing data determined to be compressible, forward error correcting the data and interleaving the data in a bit matrix memory to enhance the forward error correction. Digital information packets are formulated including a header bearing a packet number, the total packet byte count, any packet number resend request, the data byte count of the actual data and a CRC. The digital information packet is loaded onto a transmitter carousel having a fixed number of sectors. The receiver receives the data, requests resend of any packet (by number) that is defective, error corrects if necessary and sequentially loads the packet onto a receiver carousel. Packets or sequential packet groups are removed from the carousel, selectively decompressed and the data words extracted and sent to the output.

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Method and system for data transmission, using forward error correction and frame interleaving.

This invention relates generally to data transmission systems and particularly to a method of operating a high speed data transmission system that is capable of error-free transfer of data in a noisy medium or in one containing other aberrations. The inventive method will be of particular benefit when used in a cellular telephone environment.

The prior art discloses many information transmission systems. A fundamental form is a basic telephone to convey voice frequency electrical signals over a pair of wires. Information that is transmitted over telephone lines is generally less susceptible to noise, phase changes and interruptions, than is information tht is sent over a radio frequency link. Dedicated or so-called "leased lines" are telephone lines that essentially bypass the telephone switching network and are even less susceptible to noise. Accurate, high speed transfer of data in such a medium is quite realizable.

The fairly recent cellular telephone service uses radio links to interconnect mobile telephones wih other mobile telephones and with conventional telephones via a telephone switching network. Mobile telephone service involves a very hostile environment. It uses frequency modulation of an RF carrier that is susceptible to interference, noise, fading, signal loss and phase shifting. While presently analog voice signals are carried reasonably well, the analog transmission of digital data, which is readily carried out over normal telephone lines, is rendered nearly impossible due to noise and other aberrations, such as those above mentioned, in the cellular telephone medium.

There are two fundamental problems in data transmission: accuracy and speed. Conventional data transmission systems are known wherein data is formulated

into blocks or packets and some form of error protection, such as a check sum or a cyclic redundancy code (CRC), is appended to the data for providing a means at the receiver to determine whether the data has been corrupted or impaired during transmission. If an impaired packet is received, the receiver signals the transmitter to retransmit, beginning with the impaired packet.

There are well-known mathematical and physical techniques for compressing data to reduce the necessity of transmitting repetitive bit groupings. In data compression, a "compression table" (or "hash" table as it is colloquially referred to) is constructed of patterns of characters or bit groupings with the various patterns being identified. The pattern identifiers are transmitted rather than the character patterns or bit groupings themselves. These techniques can be shown to improve system throughput by allowing more data to be sent in a shorter time period and are in common usage. In the preferred embodiment, a system of data compression based upon the Lempel-Zev-Welch (LZW) compression technique is utilized. Information on LZW compression may be found in A Method for Construction of Minimum Redundancy Codes by D.A. Huffman, Proceeding of the IRE, 1952 and Pattern Matching in Strings SIAM, by D.E. Knuth, Journal on Computing, June 1977. There are many other treatises on the subject.

The technique known as forward error correction (FEC) is also known for detecting and correcting errors in data. Mathematical models by Huffman and Golay, (and others), for error correcting bit strings are known. In all of the FEC systems, the number of bytes of transmitted information is significantly increased and generally permits the detection of only a limited number of bit errors in a protected bit packet and the correction of a lesser number of bit errrs in the protected bit packet. Errors in excess of the correctable number require

retransmission. FEC systems have been sparingly used.

In Golay encoding, which is used in the invention, a check word is created to forward error correct a code word. A code word is generally the same as a data word. The term, however, is used herein to differentiate from a data word since, in the embodiment of the invention chosen for purposes of description, a 12 bit code word is equal to one and one-half 8 bit data words. A significant drawback to Golay FEC is that the size of the check word is non-linearly related to the number of bits to be forward error corrected. For example, in a system where three bits are protected, the check word size is equal to the code word size, i.e., the number of bits processed is doubled. Throughput suffers accordingly. FEC encoding in a high speed transmission system, such as one operating at 4800 Baud, is of limited use because it does not significantly decrease the need to resend data that is corrupted. For example, a noise pulse 0.1 seconds in duration will destroy or impair 480 bits. Consequently, such FEC techniques have not found favor in high speed data transmission systems operating over even moderately hostile links. Further information on FEC and Golay encoding may be found in the following: The Theory of Error - Correcting Codes by F.J. MacWilliams and N.J.A. Sloane, Amsterdam: North Holland, 1977; Analog Transmission Performance on the Switched Telecommunications Network by F.P. Duffy and J.W. Thatcher, Jr. Bell System Technical Journal, Volume 50, pgs. 1311-1347, April 1971; and Data Communications, Networks and Systems by T. Bartec, Macmillan Company, 1985.

In a data transmission system, an uncorrectable, defective bit packet received by the receiver requires that a replacement bit packet be sent by the transmitter. In most high speed systems, the transmitter sends a continuous sequence of packets. The receipt of a bad packet, and subsequent notification thereof by the

receiver, causes the transmission to be aborted, with the transmitter having to resend the bad packet and all succeeding packets. This type of operation also significantly degrades system throughput.

The present invention is specifically directed to a high speed, error-free method of data transmission in a very noisy environment, such as a cellular telephone link, but is also beneficial in land-based wire line or other transmission systems. The preferred embodiment of the invention is used with a modem that meets CCITT (Consultant Committee on International Telephone and Telegraphy) Specification V.32. The V.32 specification is currently directed to data transmission rates of 9600/4800 Baud. The inventive method is embodied in a protocol that incorporates a number of novel features including adaptive data compression, selective FEC, interleaving to expand FEC effectiveness, error protection and a data carousel for permitting retransmission of defective digital information packets by interspersing them into the normal sequence of packet transmissions. Each of the aspects of the invention is useful apart from its combination in the preferred embodiment of the invention. The preferred method also uses variable packet sizes, where the size of the bit packets is based, in part, on the rate of data input to increase data transmission. An added benefit of the inventive method is that the transmitted digital information is secure because the processing also encrypts the data.

Objects of the Invention

A principal object of the invention is to provide a method of operating a novel, high speed data transfer system.

Another object of the invention is to provide a data transmission system method having improved accuracy.

A further object of the invention is to provide a high speed, error-free data transmission system method

having improved throughput.

A still further object of the invention is to provide a high speed method of error-free transmission and reception of data over a noisy link.

Still another object of the invention is to provide a novel modem arrangement for high speed data transfer over a noisy link.

Brief Description of the Drawings

These and other objects and advantages of the invention will be apparent upon reading the following description in conjunction with the drawings, in which:

FIG. 1 is a block diagram of a transmitting and receiving system with an interconnecting link, with which the method of the invention is useful;

FIG. 2 is a block diagram of the microprocessor-based controller constructed in accordance with the invention;

FIG. 3 is a table illustrating the arrangement of code words and mating check words in a bit matrix memory of the invention;

FIG. 4 pictorially illustrates the arrangement of an interleave frame bit matrix and the patterns of scanning;

FIGS. 5A-5C are of commented flow chart for a transmitter constructed in accordance with the invention;

FIGS. 6A-6D are a commented flow chart for a receiver constructed in accordance with the invention; and

FIG. 7 illustrates the header and packet structure.

Description of the Preferred Embodiment

Referring to FIG. 1, Station A includes a data entry terminal 10 that is bidirectionally coupled to a microprocessor based controller 12 which is bidirectionally coupled to a data pump 14 that feeds a transmission link 16. These elements constitute the transmitter at Station A with controller 12 and data pump

14 comprising a modem for accepting input information, preparing it for transmission and for transmitting it over transmission link 16. At the receiver at Station B, a data pump 18 is intercoupled with transmission link 16 and supplies information to a microprocessor based controller 20 that is, in turn, coupled to a data entry terminal 22. Data pump 18 and controller 20 likewise may constitute a receiving modem. As is well known, the provision of the bidirectional paths indicates that the system operates in either direction with the transmitter operating as a transmitter for data flow in one direction and as a receiver for data flow in the opposite direction - simultaneously. Such transmitter-receivers are full duplex and are also commonly referred to as transceivers.

The data entry terminal at either Station A or Station B may comprise a keyboard, a telephone, a computer or a data file transfer system. The data pumps 14 and 18 are in all respects conventional and include analog-to-digital and digital-to-analog converters and the appropriate mechanisms for transmitting/receiving data via the transmission link 16. Thus the data pumps may include RF modulation equipment for sending the data out as modulations of an RF carrier, or telephone access equipment for telephone line communications. In the preferred embodiment of the invention, using a modem meeting standard V.32, the data pumps will also include echo cancellation apparatus.

It will be noted that the various aspects and functions of the present invention are confined to and carried out by the controller of FIG. 1. The data pump and the controller may be combined in a modem or may be physically separate units that are connectable via conventional RS232 serial ports or by any other conventional interconnection method. This modularity makes the invention useful with any modem, but should not be considered a limitation.

With reference to FIG. 2, it will be seen that the various aspects of the invention are implemented in an integrated combination of electronic circuitry and software. That is the preferred implementation, but the invention is not to be considered limited thereto. It will also be noted that the FIG. 2 showing illustrates only one-half of a full duplex system. Operation in the reverse manner, simultaneously, should be understood with transmitter and receiver functions (and input and outputs) being interchanged. It may be advantageous to consider FIGS. 5A-5C and 6A-6D, which are respective commented flow charts for the transmitter and receiver, in conjunction with the further description of FIG. 2.

An asynchronous data stream comprising digital bits of information (at a variable data rate) is applied to the transmitter input of FIG. 2. The data conventionally includes start bits and stop bits defining data words in either a continuous or a broken stream. Synchronous serial or parallel data may also be applied to the transmitter. The data words are 8 bits long and the stop and start bits are removed as the sequential data stream is loaded into memory buffers. The number of characters (8 bit data words) received during a predetermined time interval is monitored and if the data rate indicates manual input of data, such as that from a keyboard terminal, no data compression is performed. This is because data compression groups of 1000 bits or more are stored prior to performing compression and if the input data rate is slow, system throughput will be seriously degraded by waiting to accumulate data bits. An incoming character buffer is used, and when no characters are available, a bit packet is arbitrarily formed by adding orbits to completely fill the compression buffer.

The information, either compressed or uncompressed, is subjected to forward error correction and interleaving, which enhances the benefit of FEC. FEC and

interleave processing may also be turned off to increase throughput in the event that a "clean," as opposed to a noisy, transmission link is being used. This could be a pair of leased telephone lines or simply a temporary clean condition in an otherwise noisy link. The criteria for determining when FEC is turned off is in part based upon the data rate and empirical evidence. In the preferred embodiment of the invention, FEC is turned off when six consecutive error-free digital information packets are received. (A digital information packet may be between 72 and 432 bytes in length).

The FEC packets are formulated into information packet form for transmission with a header structure containing a packet identification number, packet size and data file size information. A CRC code is added for early verification of the integrity of the header structure, the FEC encoded data is added, another CRC code is appended and the completd digital information packet is transferred to a transmission packet carousel for transmission to the data pump. Since the system is a full duplex, i.e., completely bidirectional, it is capable of simultaneously transmitting and receiving at Station A, with the opposite operations being carried out for data at Station B. Controllers may be both transmitting and receiving at the same time. Incoming data from Station A is loaded into the receiver data carousel at Station B, when determined to be error-free, and subsequently "decompressed" and provided to the data entry terminal at Station B.

As mentioned, the data compression technique utilized is LZW adapted for the use of 10 and 12 bit table entries. These size entries are even numbered, which simplifies high-speed processing and enables inplementation of the compressed data with the size of the interleave frame employed. The Golay FEC, as implemented in the preferred embodiment of the invention, doubles the size of the digital data by generating a mating check word

for each code word. The FEC allows detection of 4 bit errors and the correction of 3 bit errors per code word and mating check word combination.

The invention uses an interleave frame or bit matrix memory to greatly expand the effectiveness of the FEC. Interleaving is writing information sequentially into a bit memory in one pattern and reading bits out sequentially in another pattern for transmission. While in the preferred implementation, a bit matrix memory is used with horizontal and vertical scanning for writing and reading, it should be apparent that there are other, albeit less effective ways, to interleave without a bit matrix memory. For example, address stepping with a serial memory with address points at the terminations of code word - check word combinations may be used at the cost of extra instructions per combination. Reference to FIGS. 3 and 4 discloses the preferred arrangement of code words and mating check words in the "interleave frame" (FIG. 3) and the bit positions in the matrix (FIG. 4) using hexadecimal notation.

Each interleave frame consists of a 24 bit X 24 bit memory. A plurality of interleave frames are connected in series to make up a block of 432 bytes. Here again, it will be appreciated by those skilled in the art that the actual array size of an interleave frame and the number of frames in a block are selected to optimize the throughput of the particular data transmission system. In this connection, the effectiveness of interleaving is optimized by formulating 12 bit code words (representing one and one-half words of data) and mating 12 bit check words (representing the FEC word) and writing them horizontally (in a scanning pattern) in the 24 bit X 24 bit matrix. When the bits are read out of the bit matrix memory in a vertical direction, separation of the individual bits of the code words and check words, by an amount that is related to the size of the interleave

frame, results. In a 24 bit X 24 bit arrangement, the ability to correct 3 bits in a particular code word - check word combination is thus expanded to 3 times 24. Consequently, the duration of a noise impulse that may be tolerated without requiring a resend of an information packet is multiplied twenty-four fold.

In FIG. 3, WH1 are the most significant form bits (MSB) of the first data word, WL1 the least significant form bits (LSB) of data word 1, WH2 the MSB of data word 2, WL2 the LSB of data word 2, etc. It will be seen that, in vertically (upwardly) reading out the bit matrix, the bits in any code word - check word combination are separated during transmission to significantly increase the FEC effectiveness. An added benefit of FEC coding and interleaving is in system security because information is unintelligible to an unauthorized receiver. In cellular communications in particular, this is an important characteristic. In practice a matrix rotation of 90 degrees clockwise is used to simplify operation with the interleave frame. Hence the reading in an upwardly vertical direction.

In FIG. 7, the makeup of the digital information packet structure used in the preferred embodiment is shown. The maximum total packet size is 432 bytes, although, as mentioned above, this number is not to be considered limiting. The first two bytes are labelled SOH (start of header) with the first byte being hexadecimal AA and the second byte being either hexadecimal 55 or 5A. These two bytes are selected to be unique from any other characters that may ever be encountered and are not counted in the total block byte count. The 55 hexadecimal denotes no FEC and 5A denotes FEC. The next two bytes of the header are the total byte count in the digital information packet structure or block. This is a two-byte number with the byte of lowest significance occupying the first byte position in the header and that of greater significance occupying the second byte position in the header. The

next byte identifies the block number, which in the preferred embodiment is 1 to 255. (0 is an invalid block number.) The next two bytes are the data count, that is the number of actual bytes in the data portion of the block. The next block is a NAK (numbered no acknowledgement) and constitutes a resend request to the other station to resend a particular numbered, previously transmitted digital information packet. Since each of Station A and B can transmit, they have their own transmission packet numbers. The 0 indicates "no NAK" or no request for a packet resent. The next two bytes consist of a header CRC code. The provision of a header CRC contributes to system throughput because an error received in the header saves the need for time consuming processing by immediately requesting a resend (via a NAK). The next group of bytes is variable (within the limits set for information packet or block size) and comprises the user data. The last two bytes are the packet CRC code for determining whether the packet has been received error-free.

The packets are loaded onto a transmission packet "carousel" which consists of a cyclical array of segmented memory with 16 sectors of 432 bytes each. It may be helpful to think of it as children's pony carousel with 16 ponies representing packet carriers. Packets are loaded onto the carousel and are identified by their packet numbers. When the carousel is full, the oldest packet is overwritten by the new packet being loaded on the carousel. Transmission is sequential and continuous. The transmitter is never allowed to overwrite a packet on the carousel that has not been acknowledged as being received error-free.

In the receiver, the packets are CRC code checked and forward error corrected before they are loaded onto a receiving carousel, which also has 16 sectors of 432 bytes each. First the header CRC is checked, then the packet

CRC, and FEC decoding, if used, is performed. A defective packet is not loaded on the carousel but the sector corresponding thereto is left empty. The receiver will immediately NAK (request a resend of) that packet by inserting its packet number in the next digital information packet sent to the transmitter. (If no data is available for transmission the NAK will be sent in a padded packet.) All subsequently transmitted packets are received, error checked and corrected and, if found to be error-free, loaded onto the successive sectors of the carousel following the empty sector. An error-free packet replacement for a defective packet is loaded into the empty slot corresponding to it on the carousel and only then are the higher numbered packets removed for further processing. Since the data has a specific time relationship, it is essential that packets not be removed from the carousel out of order to maintain the packet sequence. Should a subsequent NAK not result in an error-free replacement packet being received, the receiver will NAK incoming good packets to preclude the transmitter from losing data by overrunning the carousel. As in most transmitter systems, the incoming data is throttled or held up when the transmitter is in danger of falling behind. Thus, the receiver controls the transmitter, which controls the incoming data stream. In the preferred embodiment the input data rate is preferably twice the rate of the transmission link, which allows for benefits realized from data compression.

While a specific implementation of the invention has been described, it is recognized that modifications thereof will readily occur to those skilled in the art without departing from its true spirit. The invention is to be limited only as defined in the claims.

CLAIMS

1. A method of transmitting data comprising the steps of:

formulating bit packets of code words and check words, said code words defining digital information to be transmitted and said check words being formulated to forward error correct said code words;

writing the bits of said code words and of said check words into a bit memory in a first pattern;

formulating digital information packets by reading bits from said bit memory in a second pattern to separate adjacent bits in said code words and said check words; and

transmitting said digital information packets.

2. The method of claim 1 wherein said bit memory comprises a bit matrix having horizontal rows and vertical columns of bits; and wherein one of said first and second patterns encompasses sequentially scanning said horizontal rows and the other encompasses sequentially scanning said vertical columns.

3. The method of claim 2 wherein said code words comprise bits from more than one data word.

4. The method of claim 3 wherein said code words and said check words each comprise 12 bits and wherein said bit memory matrix has a size of 24 bits X 24 bits.

5. The method of claim 4, further including a plurality of said bit matrix memories and wherein said digital information packets comprise a series of said plurality of bit matrix memories.

6. A method of processing sequentially transmitted digital information packets comprising bit packets of data defining code words and forward error correcting check words that have been formed by writing to a bit memory in a first pattern and reading from said bit memory in a second pattern, comprising the steps of:

receiving and detecting said digital information

packets;

writing said digital information packets into a bit memory using said second pattern;

developing said bit packets of code words and check words from said bit memory by reading bits out of said bit memory using said first pattern; and

error correcting said code words with said check words.

7. The method of claim 6 wherein said bit memory comprises a matrix of horizontal rows and vertical columns of bits; and wherein one of said first and second patterns encompasses sequentially scanning said horizontal rows and the other encompasses sequentailly scanning said vertical columns.

8. The method of claim 7 wherein said code words comprise bits from more than one data word.

9. The method of claim 8 wherein said code words and said check words each comprise 12 bits and wherein said bit memory matrix comprises 24 bits X 24 bits.

10. The method of claim 9 wherein said digital information packets are formulated by reading a series of said transmitter bit matrix memories and further including the step of sequentially writing said digital information packets into a series of receiver bit matrix memories and sequentially reading said series of receiver bit matrix memories to develop said bit packets.

11. A method of operating a data transmission system including a transmitter and a receiver comprising the steps of: at the transmitter:

formulating code words for conveying digital information and check words for correcting errors in said code words;

writing the bits of said code words and said check words into a bit memory matrix using a first pattern;

formulating digital information packets by reading bits from said bit memory matrix using a second

pattern to separate adjacent bits in said code words and said check words;

transmitting said digital information packets; at the receiver;

receiving and detecting said transmitted digital information packets;

writing said digital information packets into a similar bit matrix memory using said second pattern;

developing said code words and said check words from said bit matrix memory by reading bits from said bit memory matrix using said first pattern; and

error correcting said code words with said check words.

12. The method of claim 11 wherein said bit memory matrices each comprise horizontal rows and vertical columns of bits; and wherein one of said first and second patterns encompasses sequentially scanning said horizontal rows and the other encompasses sequentially scanning said vertical columns.

13. The method of claim 12 wherein said code words comprise bits from more than one data word.

14. The method of claim 13 wherein said code words and said check words each comprise 12 bits and wherein said bit memory matrix comprises 24 bits X 24 bits.

15. The method of claim 14 wherein said digital information packets are formulated from a series of bit matrix memories at the transmitter and further including sequentially writing said digital information packets into a series of bit matrix memories at the receiver and sequentially reading said series of bit matrix memories at the receiver to develop said code words and check words.

16. A method of transmitting data from a transmitter to a receiver with improved throughput comprising the steps of:

formulating data into identifiable packets;

sequentially transmitting said packets to a

receiver;

checking for errors in received packets;

loading error-free packets in sequence onto a packet carousel having a fixed number of packet positions;

removing error-free packets in sequence from said carousel;

signaling the identity of a defective packet to said transmitter;

maintaining an empty position on said packet carousel for a packet found to be defective;

retaining error-free data packets in positions subsequent to said empty position on said carousel; and

retransmitting said identified packet by interspersing it in the normal sequence of transmitted packets.

17. The method of claim 16 wherein each said packet includes a header identifying the number of the packet, the number of total bytes and the number of data bytes in the packet, and error detection information.

18. The method of claim 17 including a transmitter packet carousel, further comprising the steps of:

sequentially loading numbered packets onto said transmitter packet carousel;

removing packets from said transmitter packet carousel; and

overwriting the oldest packet with a new packet when said transmitter packet carousel becomes full.

19. The method of claim 18 wherein the receiver signals the identity of a defective packet by communicating the number of the defective packet to the transmitter.

20. A method of operating a modem in a noisy medium comprising the steps of:

compressing data to reduce the need to transmit repetitive bit groupings;

forming forward error corrected bit packets of code words and check words from said compressed data;

interleaving said bit packets to said check words;

formulating digital information packets from said interleaved bit packets; and

transmitting said digital information packets to a receiver.

21. The method of claim 20 further including the steps of:

providing headers for said digital information packets that identify each packet;

transmitting said digital information packets sequentially; and

retransmitting a packet found defective upon receipt of a request therefor from said receiver by breaking into the normal sequence of transmitted packets.

22. The method of claim 21, further comprising the steps of loading said packets onto a transmitter carousel;

sequentially removing said packets for transmission; and

overwriting the oldest packet on the carousel with a new packet when the carousel is full.

23. The method of claim 22, further comprising the steps of:

loading received error-free packets onto a receiver carousel;

removing error-free packets from the receiver carousel in sequence;

holding open positions on the receiver carousel for defective packets; and

holding packets, in positions subsequent to an open position, on the receiver carousel.

24. A method of operating a high speed modem over a noisy link to increase throughput of data from a transmitter to a receiver comprising the steps of:

selectively compressing data to reduce the need to transmit repetitive bit groupings;

formulating forward error corrected bit packets of code words and check words from said selectively compressed data;

interleaving said bit packets to separate adjacent bits of said code words and said check words;

formulating digital information packets from said interleaved bit packets with a header including packet identification;

error protecting said digital information packets;

loading said digital information packets onto a transmitter packet carousel;

transmitting said digital information packets from said carousel in sequence;

terminating forward error correction during noise-free digital information periods on the link; and

retransmitting a defective digital information packet by interspersing it into the sequence of packets loaded onto the carousel.

25. The method of claim 24 wherein said interleaved bit packets are formed by writing the bits of said code words and said check words into a bit memory matrix in a first pattern and reading said bits from said bit memory matrix in a second pattern.

26. The method of claim 25 wherein there are a plurality of bit memory matrices, with each said digital information packet comprising a series of said memory matrices and wherein said code words comprise bits from more than one data word.

27. The method of claim 26 wherein said forward error correction utilizes Golay encoding and wherein compression is based upon Lempel-Zev-Welch techniques adapted for 10 to 12 bit strings.

28. The method of claim 27 wherein said digital information packets are of variable length and wherein

each header includes information as to the length of its associated digital information packet.

29. A microprocessor based data transfer system comprising:

a source of data;

means for compressing data from said source;

means for forward error correcting said compressed data;

interleave means for separating adjacent bits in said forward error corrected data; and

means for sequentially transmitting said interleaved data.

30. The system of claim 29 further including means for arranging said interleaved data in packets and means for error protecting said packets.

31. The system of claim 30 further including packet carousel means and means for loading said error protected packets onto said packet carousel means for sequential transmission.

32. The system of claim 31 further including means for numbering said protected packets and further including means for retransmitting a defective numbered packet by interspersing it in the sequence of transmission of error protected packets.

33. The system of claim 32 further including means for monitoring the rate of said data from said source and means for selectively disabling said compression means based upon said rate.

34. The system of claim 33 further including means for selectively disabling said forward error correction based upon error free reception of said error protected packets.

35. A high speed microprocessor based data transfer system comprising:

a transmitter and a receiver;

means for supplying serial data to said

transmitter;

means for selectively compressing said serial data depending upon the rate of said serial data;

means for forming said data into a plurality of code word and mating check word combinations for forward error correcting said data;

means for interleaving said forward error corrected data to separate adjacent bits in said code word and check word combinations;

means for formulating error protected packets of said interleaved data;

means for loading said error protected packets onto a transmitter packet carousel; and

means for sequentially transmitting said error protected packets from said transmitter packet carousel to said receiver.

36. The system of claim 35 wherein said error protected packets are numbered and further including:

means for detecting defective packets at said receiver;

means for indicating the number of a defective packet to said transmitter;

means for loading error free detected packets onto a receiver packet carousel; and

means for retransmitting a defective packet by interspersing it in the sequence of transmitted packets.

37. The system of claim 36 wherein said packet carousels each comprise a fixed number of sectors and wherein said receiver skips a sector corresponding to a received defective packet and holds subsequently received error free packets on said receiver packet carousel until an error free replacement for said defective packet is received and loaded in said skipped sector.

FIG.1

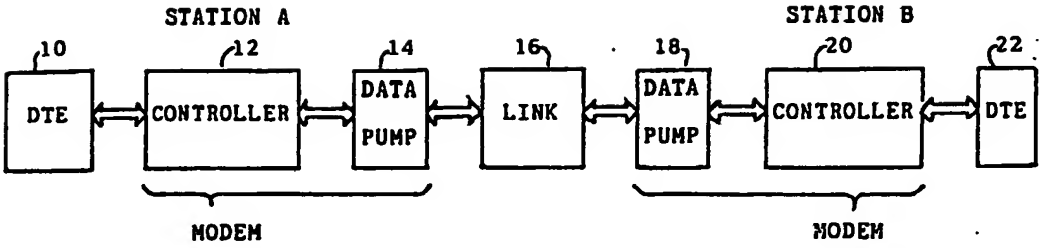



FIG.3

| | | | | |
|---|---|---|---|---|
| WH1 | WL1 | WH2 | (12 bits) | (12-bit calculated check word) |
| WL2 | WH3 | WL3 | (12 bits) | (12-bit calculated check word) |
| WH4 | WL4 | WH5 | (12 bits) | (12-bit calculated check word) |
| WL5 | WH6 | WL6 | (12 bits) | (12-bit calculated check word) |
| WH7 | WL7 | WH8 | (12 bits) | (12-bit calculated check word) |
| WL8 | WH9 | WL9 | (12 bits) | (12-bit calculated check word) |
| WHA | WLA | WHB | (12 bits) | (12-bit calculated check word) |
| WLB | WHC | WLC | (12 bits) | (12-bit calculated check word) |
| WHD | WLD | WHE | (12 bits) | (12-bit calculated check word) |
| WLE | WHF | WLF | (12 bits) | (12-bit calculated check word) |

FIG.4

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 01 | 02 | 03 | . . . . . | | 16 | 17 | 18 |
| 19 | 1A | 1B | | | 2E | 2F | 30 |
| 31 | 32 | 33 | | | 46 | 47 | 48 |
| . | | | | | | | . |
| . | | | | | | | . |
| . | | | | | | | . |
| . | | | | | | | . |
| . | | | | | | | . |
| 1F9 | 1FA | 1FB | | | 20E | 20F | 210 |
| 211 | 212 | 213 | | | 226 | 227 | 228 |
| 229 | 22A | 22B | . . . . . | | 23E | 23F | 240 |

Write sequentially scanning from left to right.

01, 02, 03,...23E, 23F, 240.

Read sequentially scanning from bottom to top.

229, 211, 1F9...48, 30, 18.

FIG.7

| SOH 01 | SOH 02 | BYTE LOW | CNT HI | BLOCK NUM | DATA LOW | CNT HT | NAK or 0 | HDR LOW | CRC HI | USER DATA AREA VARIABLE SIZE | HDR LOW | CRC HI |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

FIG.2

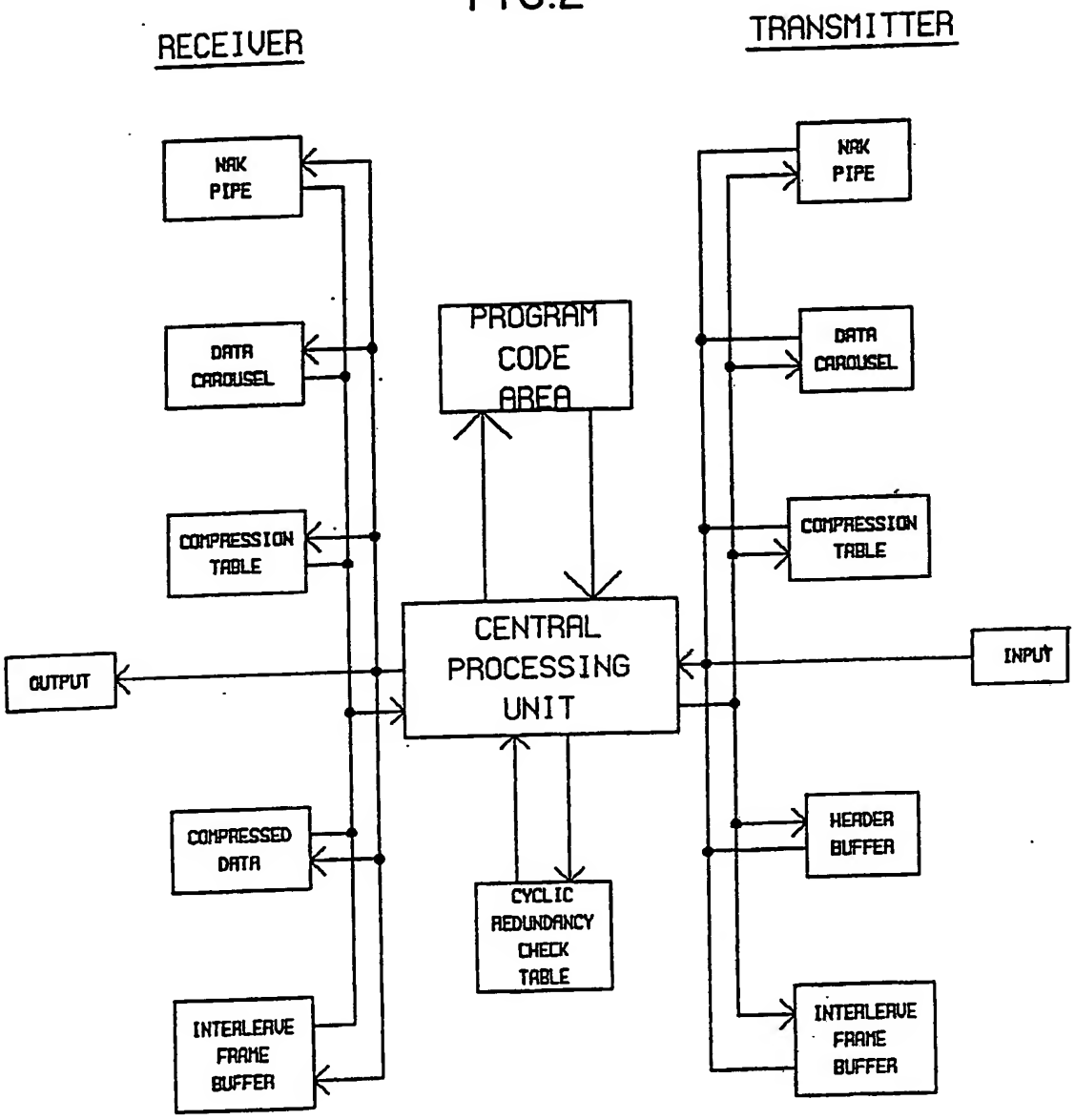

RECEIVER
TRANSMITTER
NAK PIPE
DATA CAROUSEL
COMPRESSION TABLE
OUTPUT
COMPRESSED DATA
INTERLEAVE FRAME BUFFER
PROGRAM CODE AREA
CENTRAL PROCESSING UNIT
CYCLIC REDUNDANCY CHECK TABLE
NAK PIPE
DATA CAROUSEL
COMPRESSION TABLE
INPUT
HEADER BUFFER
INTERLEAVE FRAME BUFFER

FIG.5A

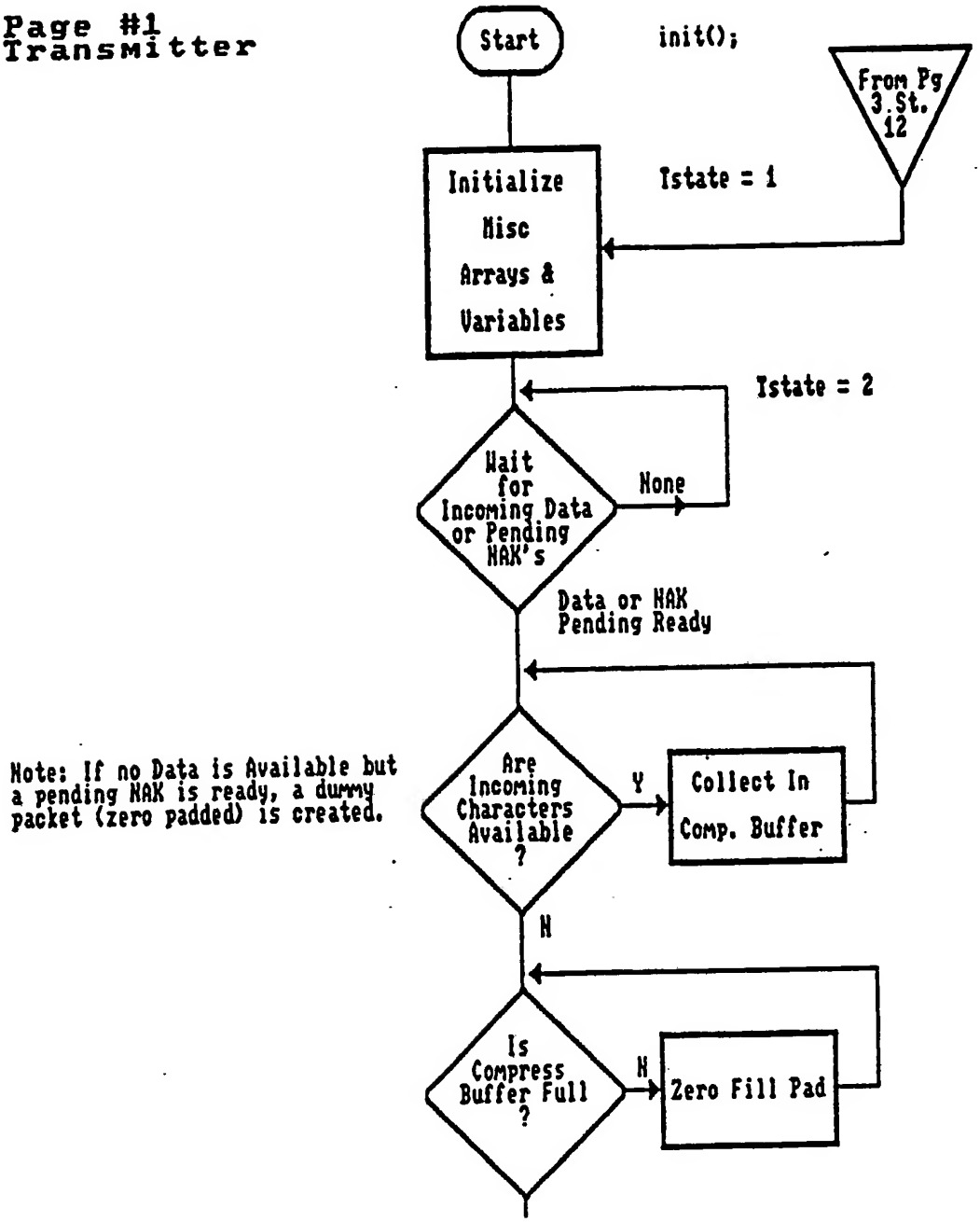

Page #1
Transmitter
Start
init();
From Pg 3.St. 12
Initialize Misc Arrays & Variables
Istate = 1
Istate = 2
Wait for Incoming Data or Pending NAK's
None
Data or NAK Pending Ready
Are Incoming Characters Available ?
Y
Collect In Comp. Buffer
N
Is Compress Buffer Full ?
N
Zero Fill Pad
Note: If no Data is Available but a pending NAK is ready, a dummy packet (zero padded) is created.

FIG.5A CONT.'

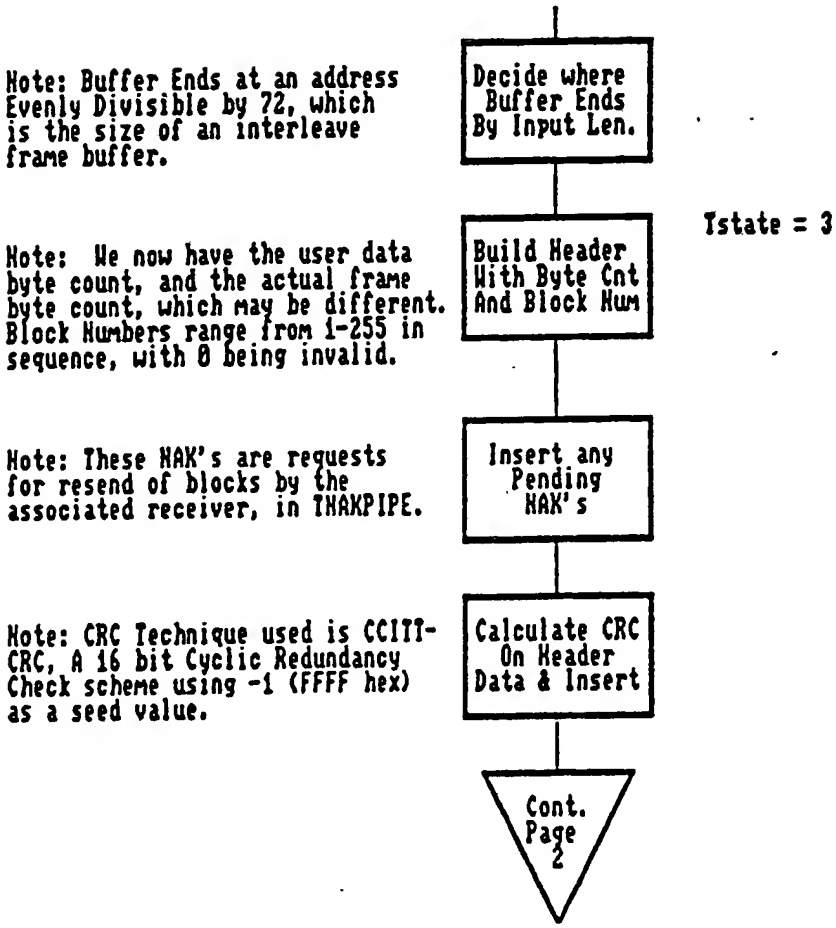
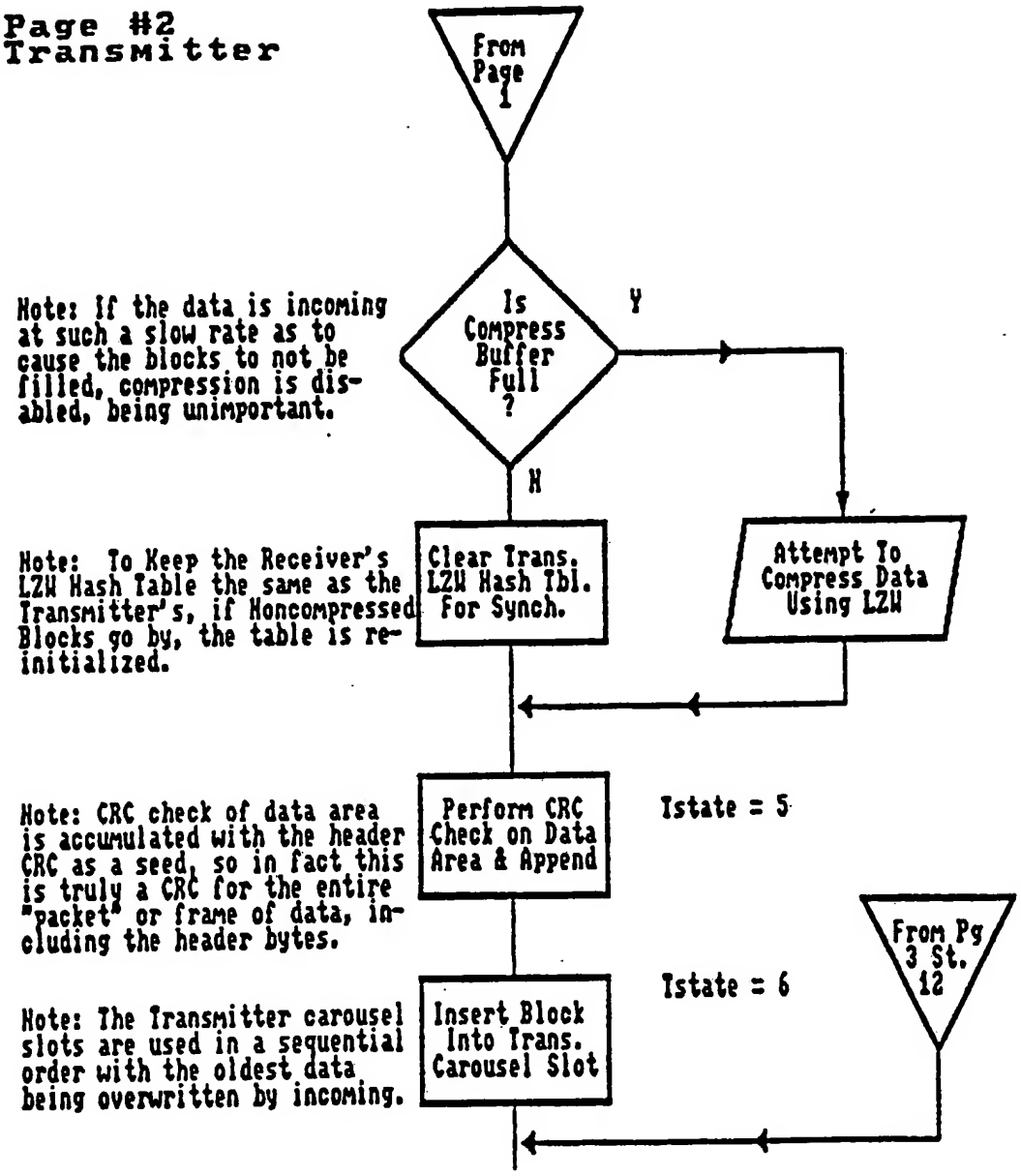

Note: Buffer Ends at an address Evenly Divisible by 72, which is the size of an interleave frame buffer.
Decide where Buffer Ends By Input Len.
Tstate = 3
Note: We now have the user data byte count, and the actual frame byte count, which may be different. Block Numbers range from 1-255 in sequence, with 0 being invalid.
Build Header With Byte Cnt And Block Num
Note: These NAK's are requests for resend of blocks by the associated receiver, in THAKPIPE.
Insert any Pending NAK's
Note: CRC Technique used is CCITT-CRC, A 16 bit Cyclic Redundancy Check scheme using -1 (FFFF hex) as a seed value.
Calculate CRC On Header Data & Insert
Cont. Page 2

FIG.5B


Page #2
Transmitter
From Page 1
Is Compress Buffer Full ?
Y
N
Note: If the data is incoming at such a slow rate as to cause the blocks to not be filled, compression is disabled, being unimportant.
Clear Trans. LZW Hash Tbl. For Synch.
Attempt To Compress Data Using LZW
Note: To Keep the Receiver's LZW Hash Table the same as the Transmitter's, if Noncompressed Blocks go by, the table is reinitialized.
Perform CRC Check on Data Area & Append
Istate = 5
Note: CRC check of data area is accumulated with the header CRC as a seed, so in fact this is truly a CRC for the entire "packet" or frame of data, including the header bytes.
From Pg 3 St. 12
Istate = 6
Insert Block Into Trans. Carousel Slot
Note: The Transmitter carousel slots are used in a sequential order with the oldest data being overwritten by incoming.

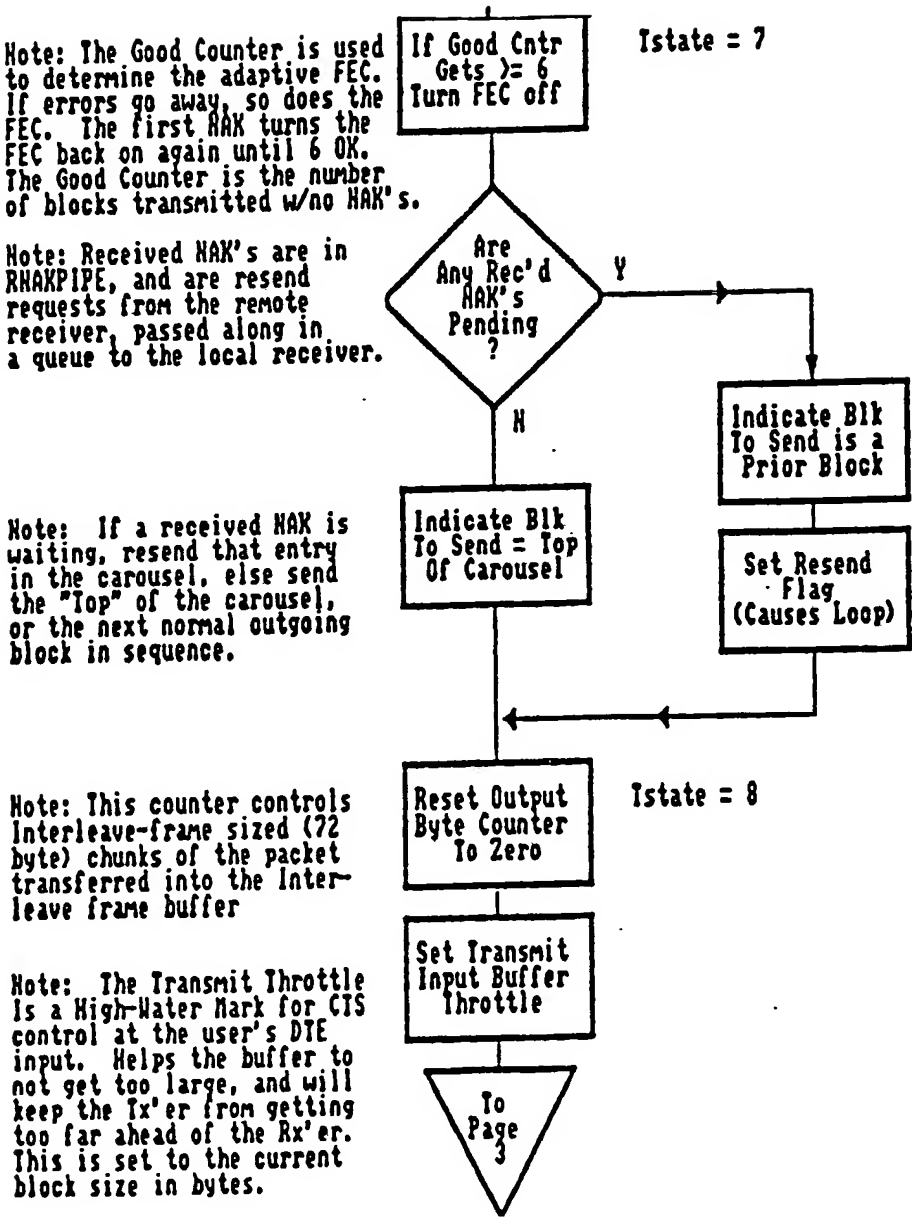
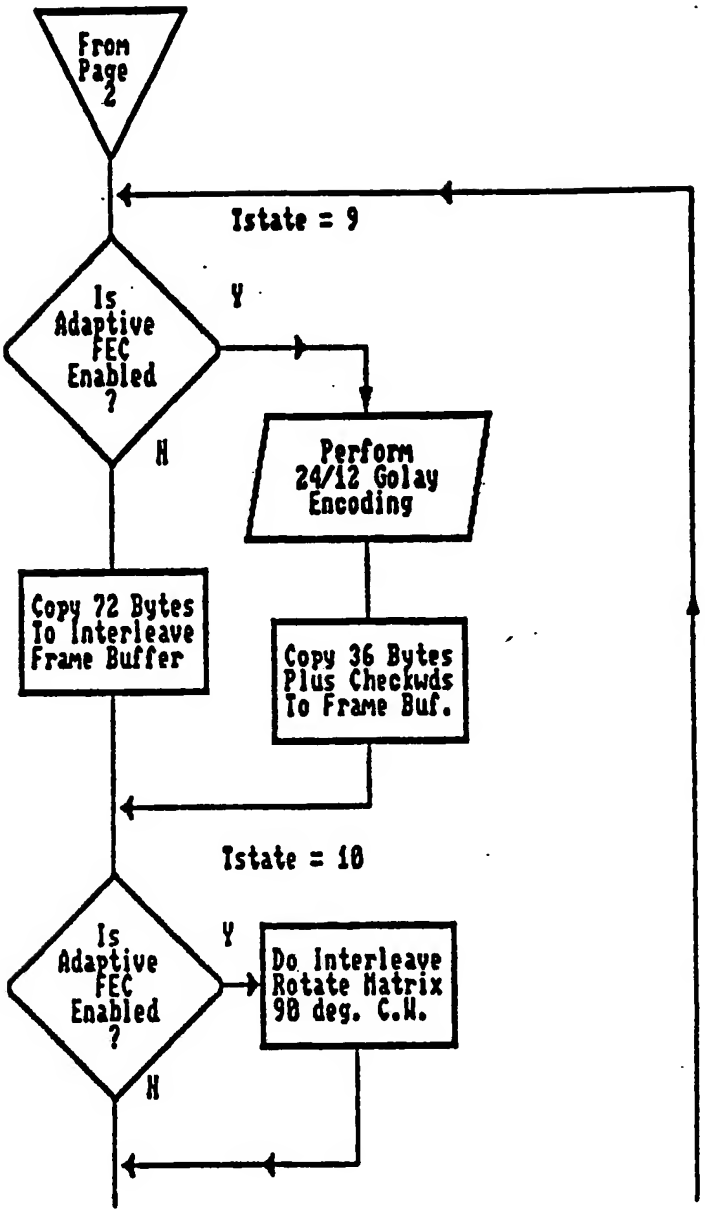

If Good Cntr Gets >= 6 Turn FEC off
Istate = 7
Are Any Rec'd NAK's Pending ?
Y
N
Indicate Blk To Send is a Prior Block
Set Resend Flag (Causes Loop)
Indicate Blk To Send = Top Of Carousel
Reset Output Byte Counter To Zero
Istate = 8
Set Transmit Input Buffer Throttle
To Page 3
Note: The Good Counter is used to determine the adaptive FEC. If errors go away, so does the FEC. The first NAK turns the FEC back on again until 6 OK. The Good Counter is the number of blocks transmitted w/no NAK's.
Note: Received NAK's are in RNAKPIPE, and are resend requests from the remote receiver, passed along in a queue to the local receiver.
Note: If a received NAK is waiting, resend that entry in the carousel, else send the "Top" of the carousel, or the next normal outgoing block in sequence.
Note: This counter controls Interleave-frame sized (72 byte) chunks of the packet transferred into the Interleave frame buffer
Note: The Transmit Throttle Is a High-Water Mark for CTS control at the user's DTE input. Helps the buffer to not get too large, and will keep the Tx'er from getting too far ahead of the Rx'er. This is set to the current block size in bytes.

FIG. 5B CONT.'

FIG.5C

Page #3
Transmitter



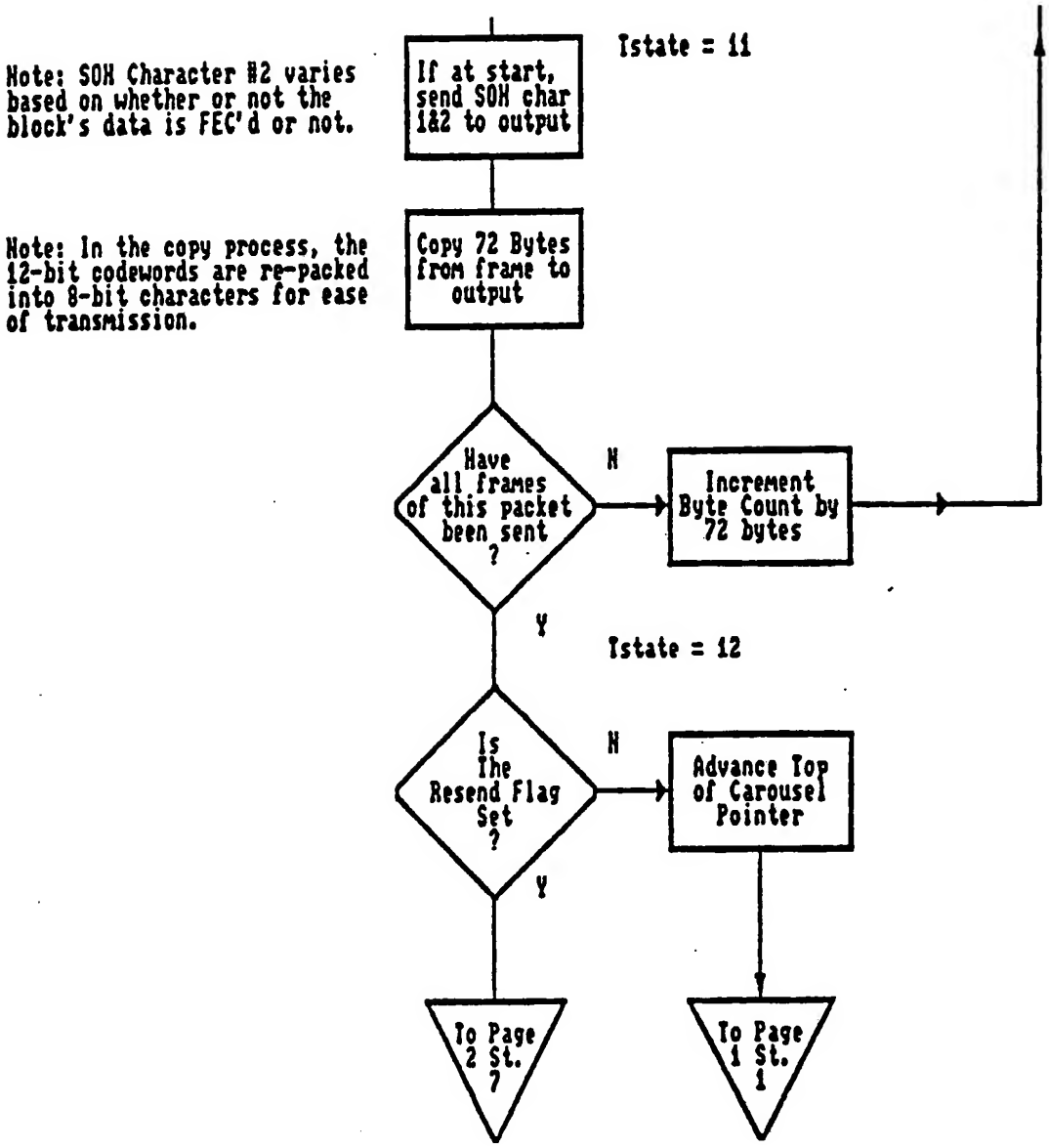
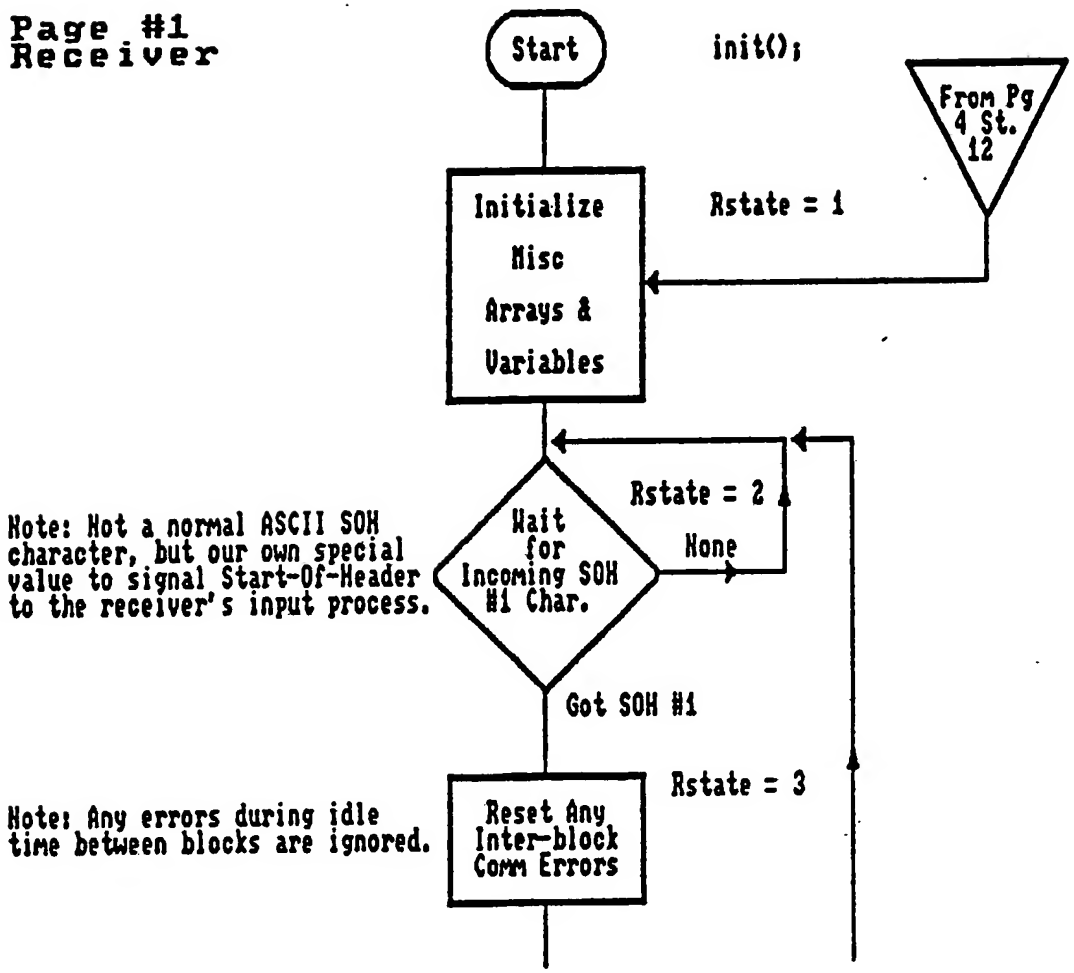

Note: SOH Character #2 varies based on whether or not the block's data is FEC'd or not.
If at start, send SOH char 1&2 to output
Istate = 11
Note: In the copy process, the 12-bit codewords are re-packed into 8-bit characters for ease of transmission.
Copy 72 Bytes from frame to output
Have all frames of this packet been sent ?
N
Increment Byte Count by 72 bytes
Y
Istate = 12
Is The Resend Flag Set ?
N
Advance Top of Carousel Pointer
Y
To Page 2 St. 7
To Page 1 St. 1

FIG.5C CONT.'

FIG.6A


Page #1
Receiver
Start
init();
From Pg 4 St. 12
Initialize Misc Arrays & Variables
Rstate = 1
Wait for Incoming SOH #1 Char.
Rstate = 2
None
Got SOH #1
Rstate = 3
Reset Any Inter-block Comm Errors
Note: Not a normal ASCII SOH character, but our own special value to signal Start-Of-Header to the receiver's input process.
Note: Any errors during idle time between blocks are ignored.

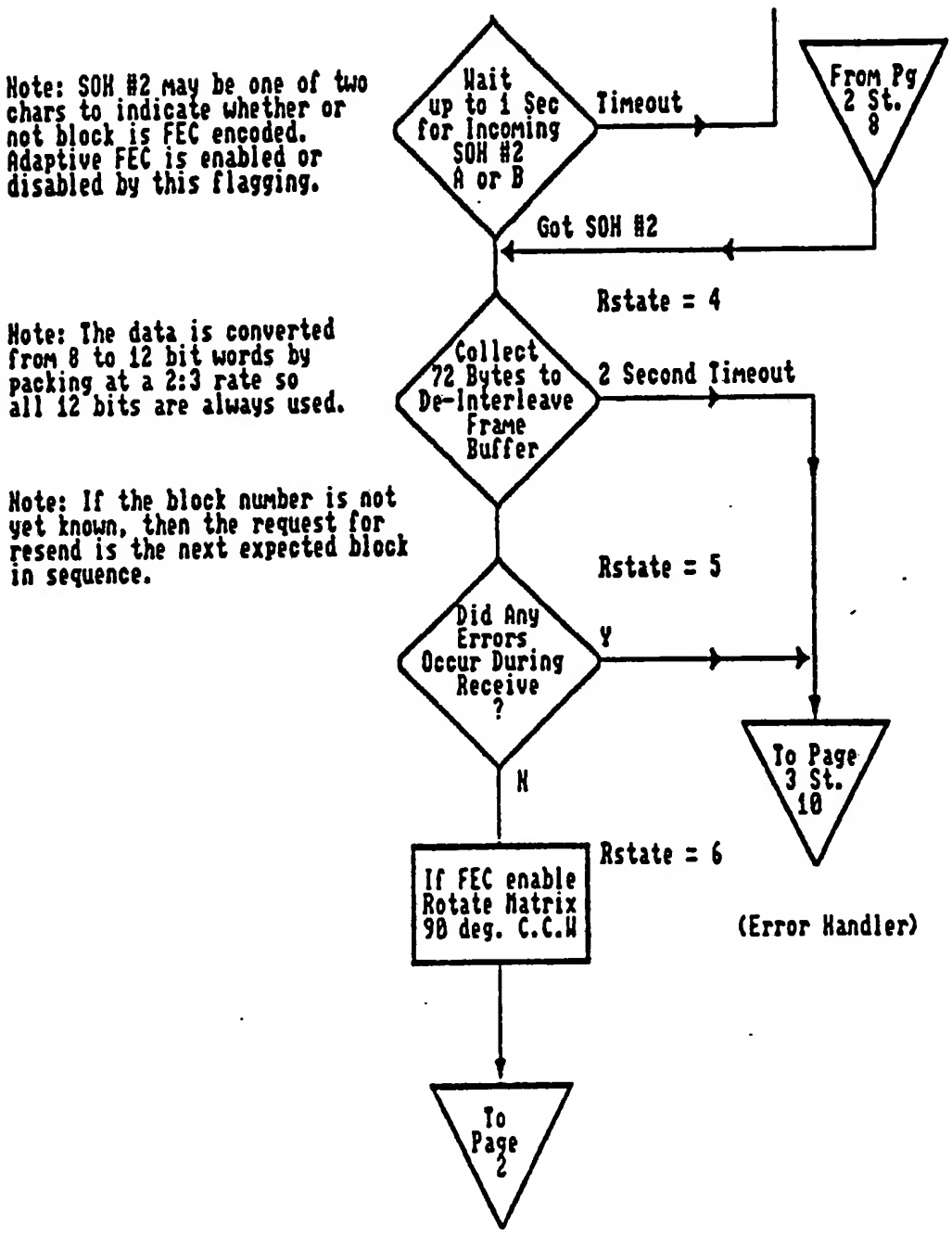
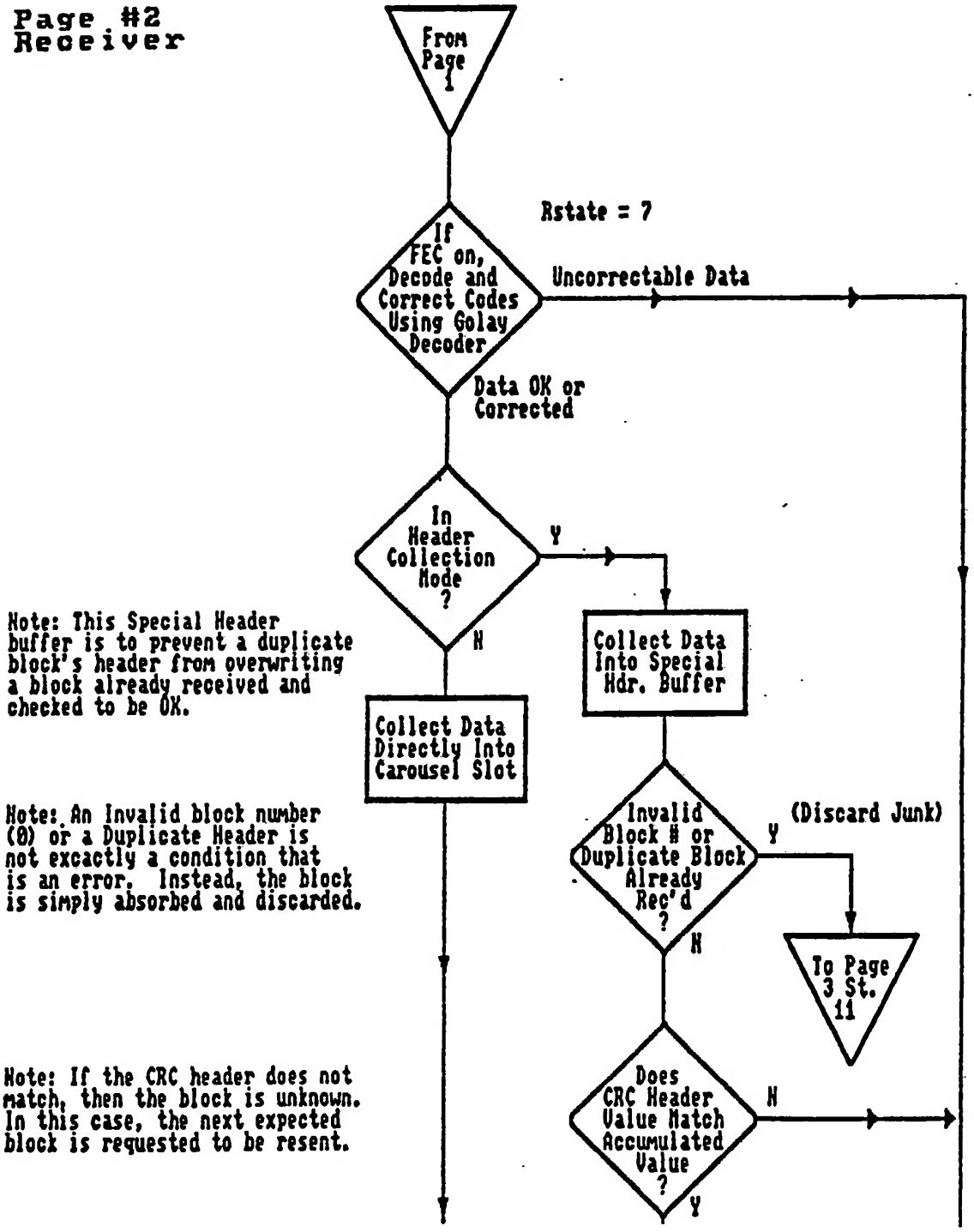

Note: SOH #2 may be one of two chars to indicate whether or not block is FEC encoded. Adaptive FEC is enabled or disabled by this flagging.
Wait up to 1 Sec for Incoming SOH #2 A or B
Timeout
From Pg 2 St. 8
Got SOH #2
Rstate = 4
Note: The data is converted from 8 to 12 bit words by packing at a 2:3 rate so all 12 bits are always used.
Collect 72 Bytes to De-Interleave Frame Buffer
2 Second Timeout
Note: If the block number is not yet known, then the request for resend is the next expected block in sequence.
Rstate = 5
Did Any Errors Occur During Receive ?
Y
N
To Page 3 St. 10
(Error Handler)
Rstate = 6
If FEC enable Rotate Matrix 90 deg. C.C.W
To Page 2

FIG.6A CONT.'

FIG.6B


Page #2
Receiver
From Page 1
Rstate = 7
If FEC on, Decode and Correct Codes Using Golay Decoder
Uncorrectable Data
Data OK or Corrected
In Header Collection Mode ?
Y
N
Collect Data Into Special Hdr. Buffer
Collect Data Directly Into Carousel Slot
Invalid Block # or Duplicate Block Already Rec'd ?
(Discard Junk)
Y
N
To Page 3 St. 11
Does CRC Header Value Match Accumulated Value ?
N
Y
Note: This Special Header buffer is to prevent a duplicate block's header from overwriting a block already received and checked to be OK.
Note: An Invalid block number (0) or a Duplicate Header is not exactly a condition that is an error. Instead, the block is simply absorbed and discarded.
Note: If the CRC header does not match, then the block is unknown. In this case, the next expected block is requested to be resent.

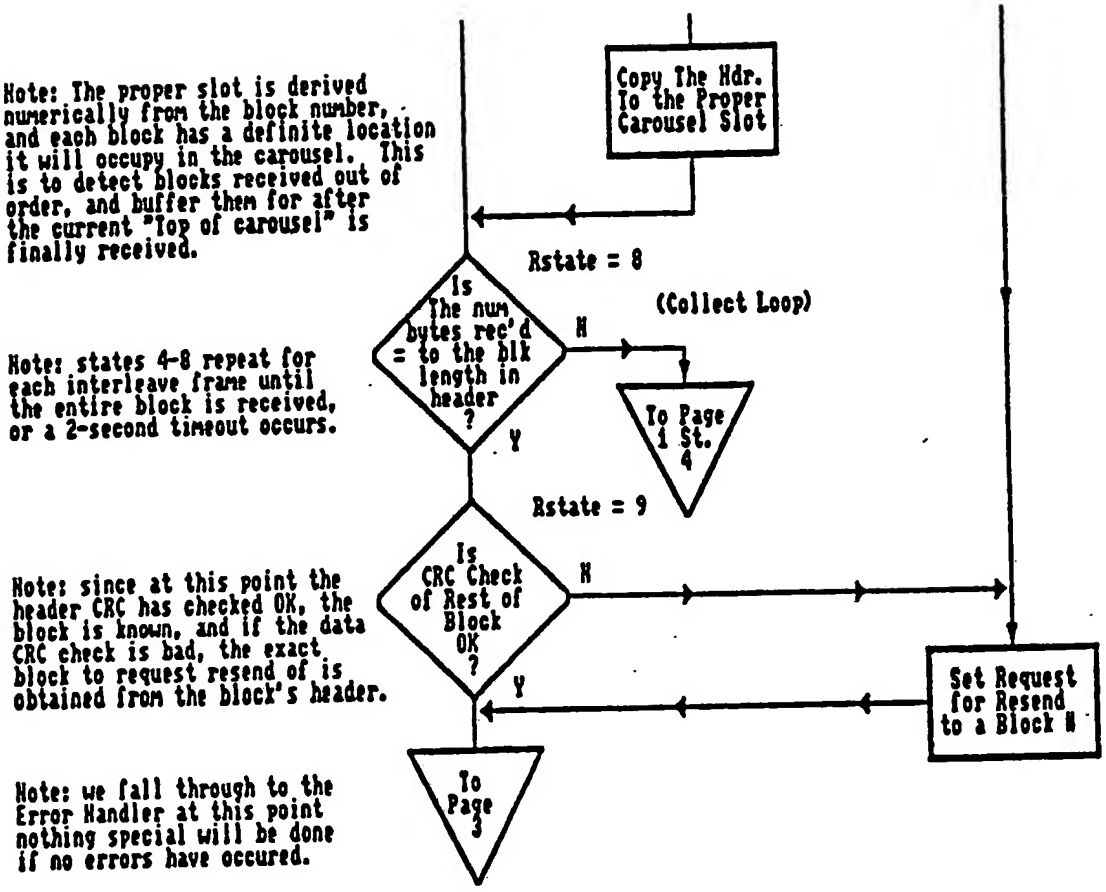
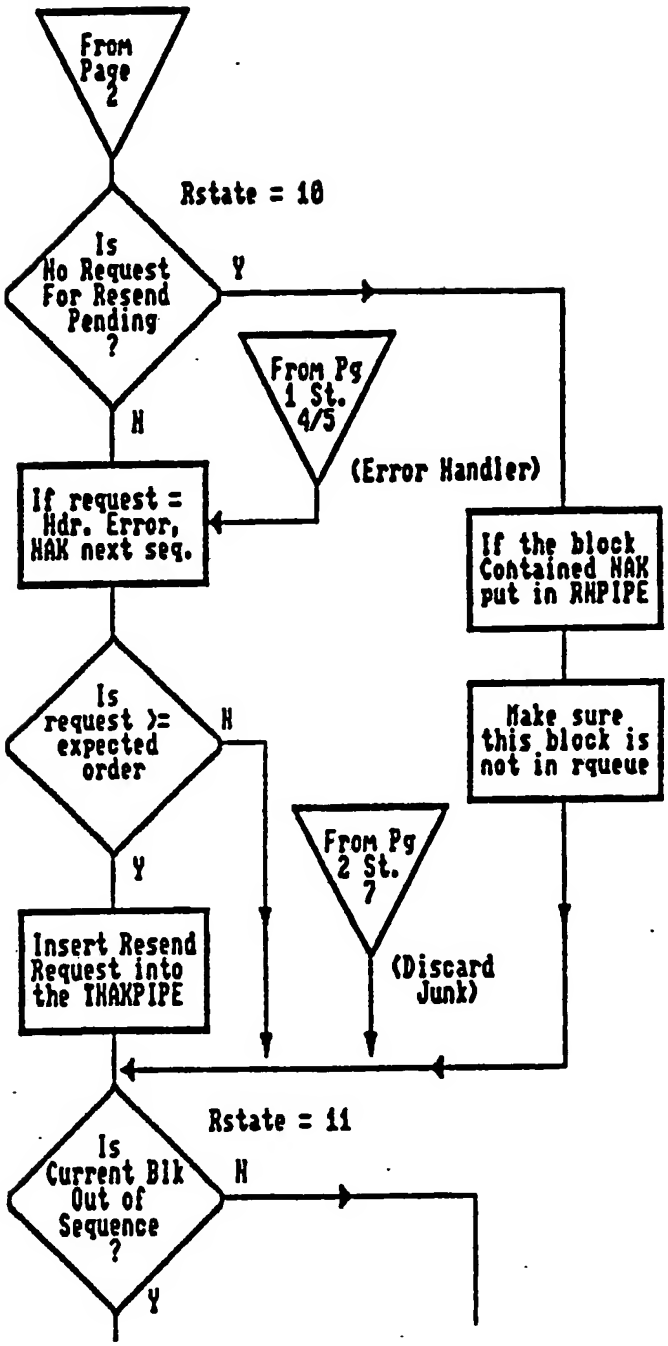

Note: The proper slot is derived numerically from the block number, and each block has a definite location it will occupy in the carousel. This is to detect blocks received out of order, and buffer them for after the current "Top of carousel" is finally received.
Copy The Hdr. To the Proper Carousel Slot
Rstate = 8
(Collect Loop)
Is The num bytes rec'd = to the blk length in header ?
N
Y
To Page 1 St. 4
Note: states 4-8 repeat for each interleave frame until the entire block is received, or a 2-second timeout occurs.
Rstate = 9
Is CRC Check of Rest of Block OK ?
N
Y
Set Request for Resend to a Block N
Note: since at this point the header CRC has checked OK, the block is known, and if the data CRC check is bad, the exact block to request resend of is obtained from the block's header.
To Page 3
Note: we fall through to the Error Handler at this point nothing special will be done if no errors have occured.

FIG.6B CONT.'

FIG.6C

Page #3
Receiver




Note: If request is less than the current order, then it is a duplicate of a block already processed and moved out of the carousel. It is ignored.

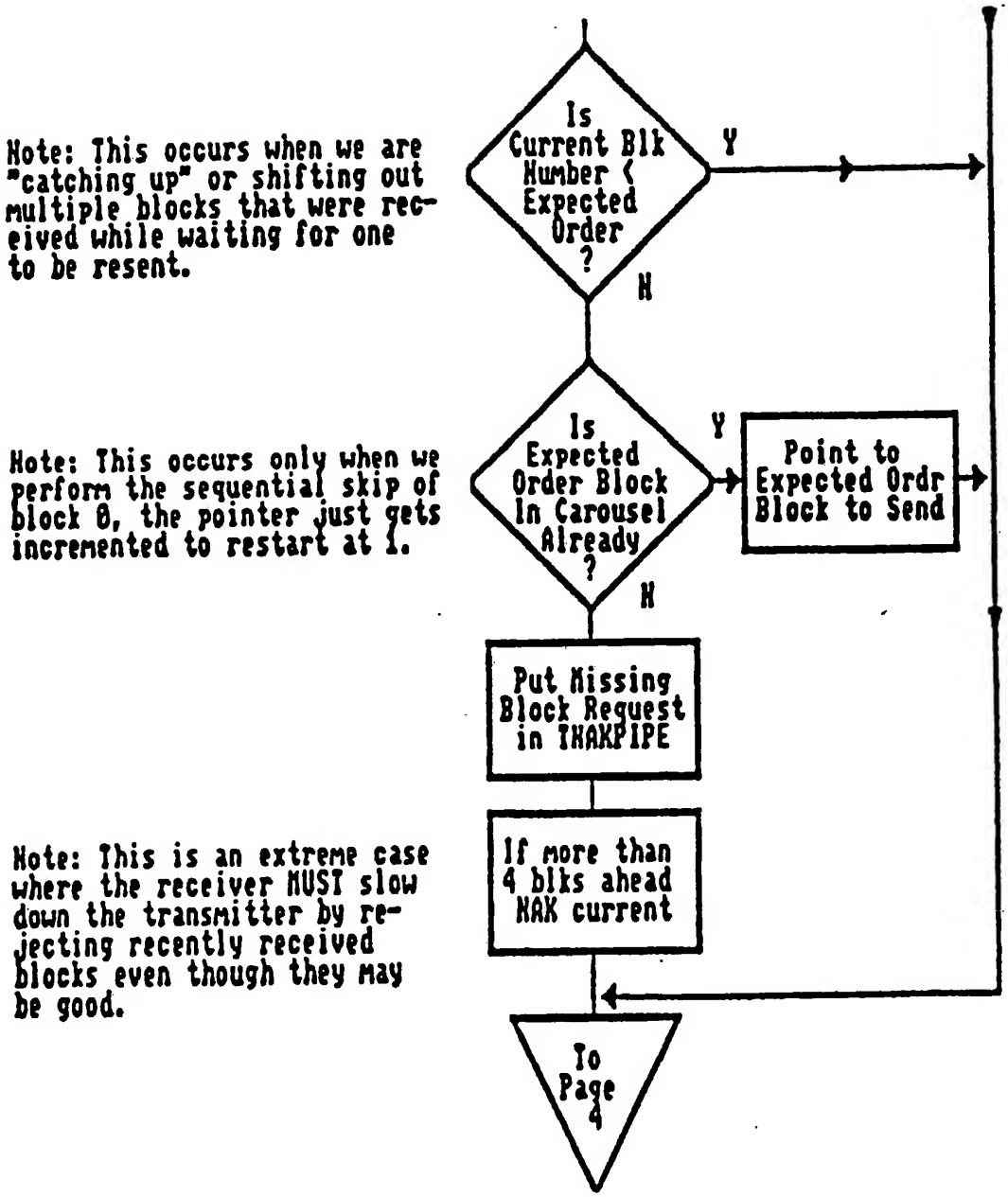
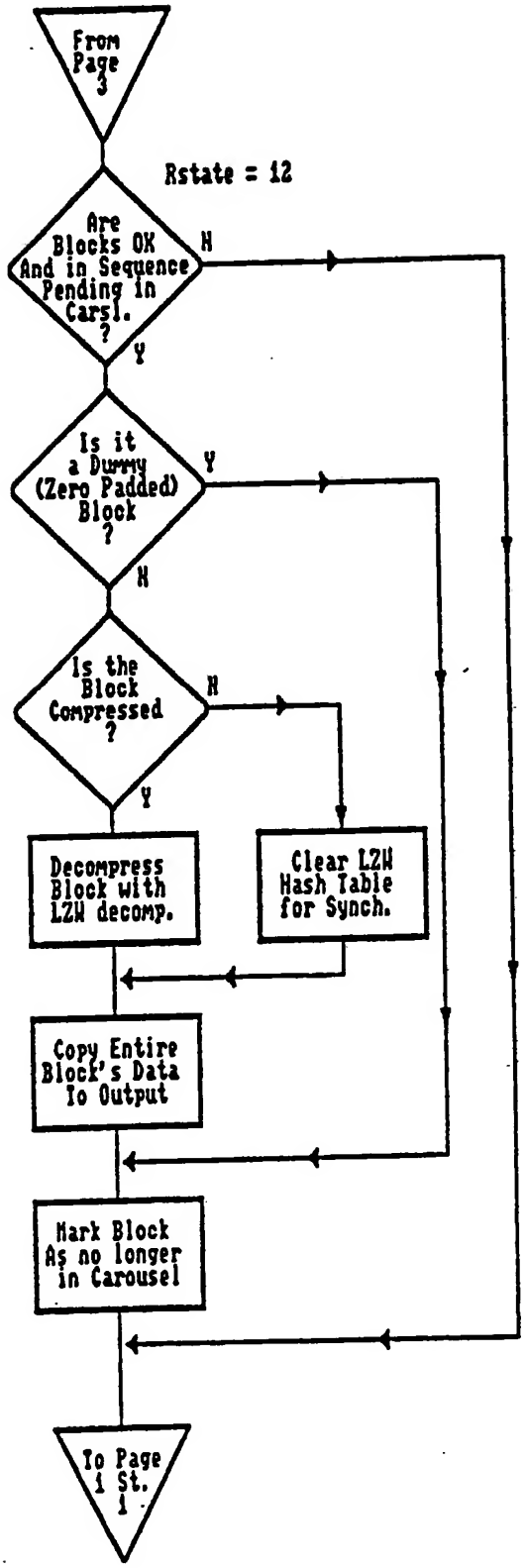

Note: This occurs when we are "catching up" or shifting out multiple blocks that were received while waiting for one to be resent.
Is Current Blk Number < Expected Order ?
Y
N
Note: This occurs only when we perform the sequential skip of block 0, the pointer just gets incremented to restart at 1.
Is Expected Order Block In Carousel Already ?
Y
Point to Expected Ordr Block to Send
N
Put Missing Block Request in THAKPIPE
Note: This is an extreme case where the receiver MUST slow down the transmitter by rejecting recently received blocks even though they may be good.
If more than 4 blks ahead NAK current
To Page 4

FIG.6C CONT.'

FIG. 6D

Page #4
Receiver



# INTERNATIONAL SEARCH REPORT

International Application No PCT/US 89/05485

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: H 04 L 1/00

## II. FIELDS SEARCHED

Minimum Documentation Searched [7]

| Classification System [8] | Classification Symbols |
|---|---|
| IPC[5] | H 04 L |

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [9]

## III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

| Category [10] | Citation of Document, [11] with indication, where appropriate, of the relevant passages [12] | Relevant to Claim No. [13] |
|---|---|---|
| X | WO, A, 86/05339 (BRITISH TELECOM) 12 September 1986 see page 2, lines 11-26; page 11, lines 15-21; figure 1 | 1,6,11,16, 20,24 |
| A | | 21-23,29-32,35-37 |
| Y | EP, A, 0239453 (CIMSA SINTRA) 30 September 1987 see column 1, lines 40-54; column 5, lines 25-30 | 1 |
| A | | 6,11,20,24, 29,30,35 |
| Y | IEEE Communications Magazine, volume 21, no. 1, January 1983, IEEE, (New York, US), V.K. Bhargava: "Forward error correction schemes for digital communications", pages 11-19, see page 15, left-hand column, lines 31-39; figure 1 | 1 |
| A | | 27,30 |

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

## IV. CERTIFICATION

| Date of the Actual Completion of the International Search | Date of Mailing of this International Search Report |
|---|---|
| 20th March 1990 | 24.04.90 |
| **International Searching Authority** | **Signature of Authorized Officer** |
| EUROPEAN PATENT OFFICE | F.W. HECK |

International Application No. PCT/US 89/05485

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

| Category * | Citation of Document, with indication, where appropriate, of the relevant passages | Relevant to Claim No |
|---|---|---|
| A | Computer Communication Review, (ACM Press: Proceedings of the ACM SIGCOMM '87 Workshop), volume 17, no. 5, 11-13 August 1987, Special Issue, ACM, (New York, N.Y., US), S. Mohan et al.: "Efficient point-to-point and point-to-multipoint selective- repeat ARQ schemes with multiple retransmissions: a throughput analysis", pages 49-57 see page 49, right-hand column, lines 16-29 | 16,18,19, 21-23,31, 36,37 |

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# ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8905485 SA 32975

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 11/04/90
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| WO-A- 8605339 | 12-09-86 | AU-A- 5519886 | 24-09-86 |
| | | EP-A- 0216813 | 08-04-87 |
| | | JP-T- 62502160 | 20-08-87 |
| | | US-A- 4829526 | 09-05-89 |
| EP-A- 0239453 | 30-09-87 | FR-A- 2595522 | 11-09-87 |
| | | JP-A- 62277827 | 02-12-87 |
| | | US-A- 4803685 | 07-02-89 |